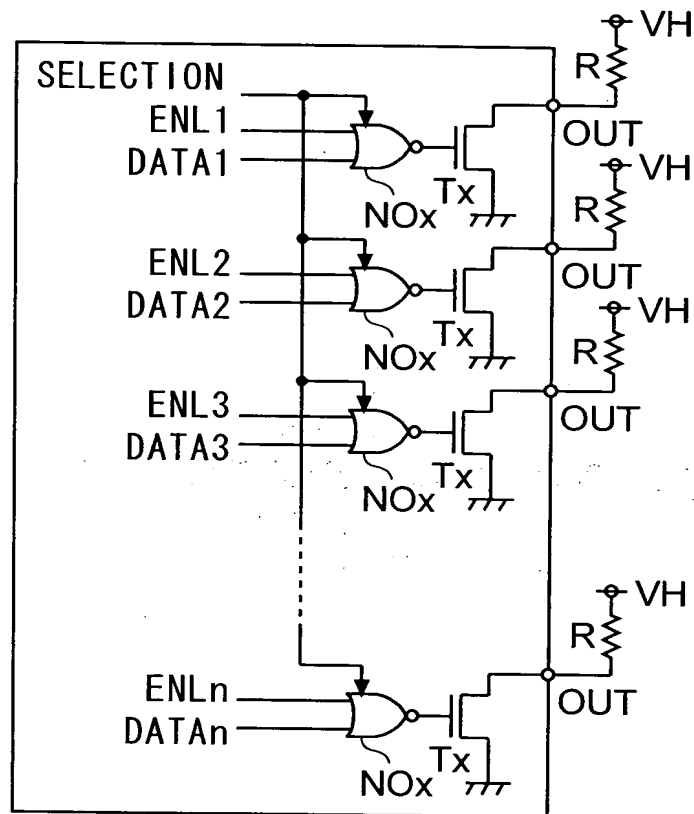


[illegible]

The circuit diagram shows a 1-bit DAC. It features a differential pair of NMOS transistors, \$M_{1a}\$ and \$M_{1b}\$, whose gates are connected to a common input labeled 'DATA ENL'. The sources of these transistors are connected to ground. The drains are connected to a current mirror load consisting of two PMOS transistors, \$M_{2a}\$ and \$M_{2b}\$. The gates of \$M_{2a}\$ and \$M_{2b}\$ are connected to a common bias voltage 'VDD'. The drain of \$M_{2a}\$ is connected to the drain of \$M_{1a}\$ and to the gate of \$M_{2b}\$. The drain of \$M_{2b}\$ is connected to the drain of \$M_{1b}\$ and to the gate of \$M_{2a}\$. The output of the DAC is taken from the drain of \$M_{1a}\$, which is also connected to a load capacitor 'C' and a load resistor 'R1a'. The other end of the load capacitor 'C' and load resistor 'R1a' is connected to ground. The output signal is labeled 'OUT'.

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FIG.3

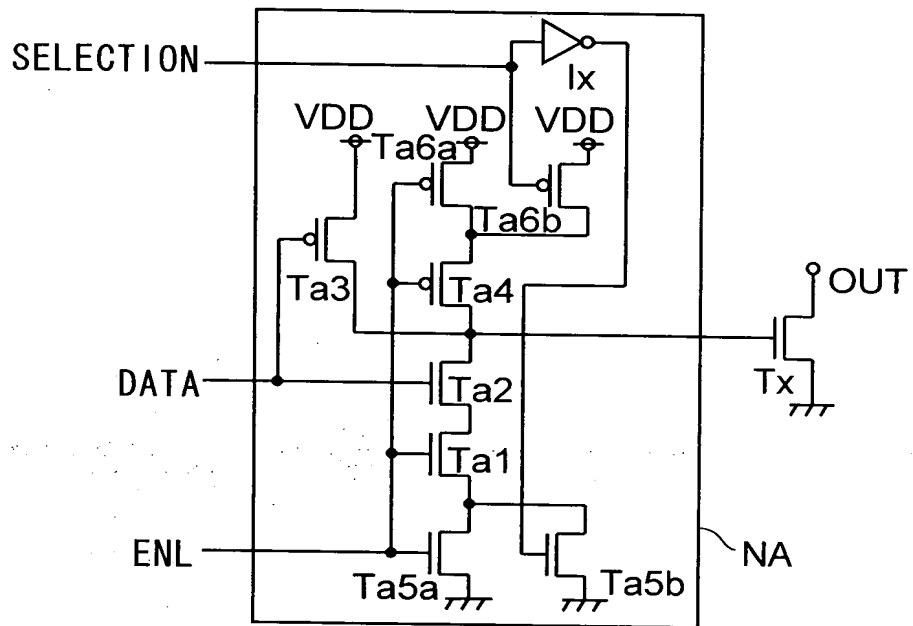


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FIG.4

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FIG.5

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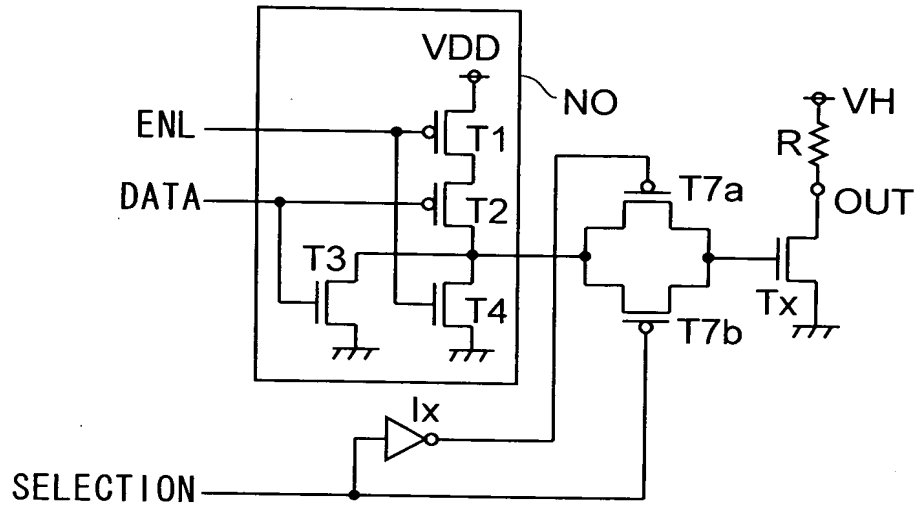
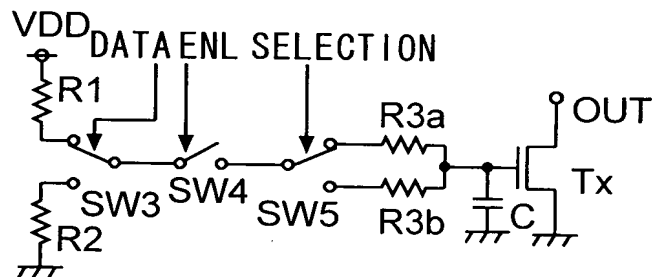
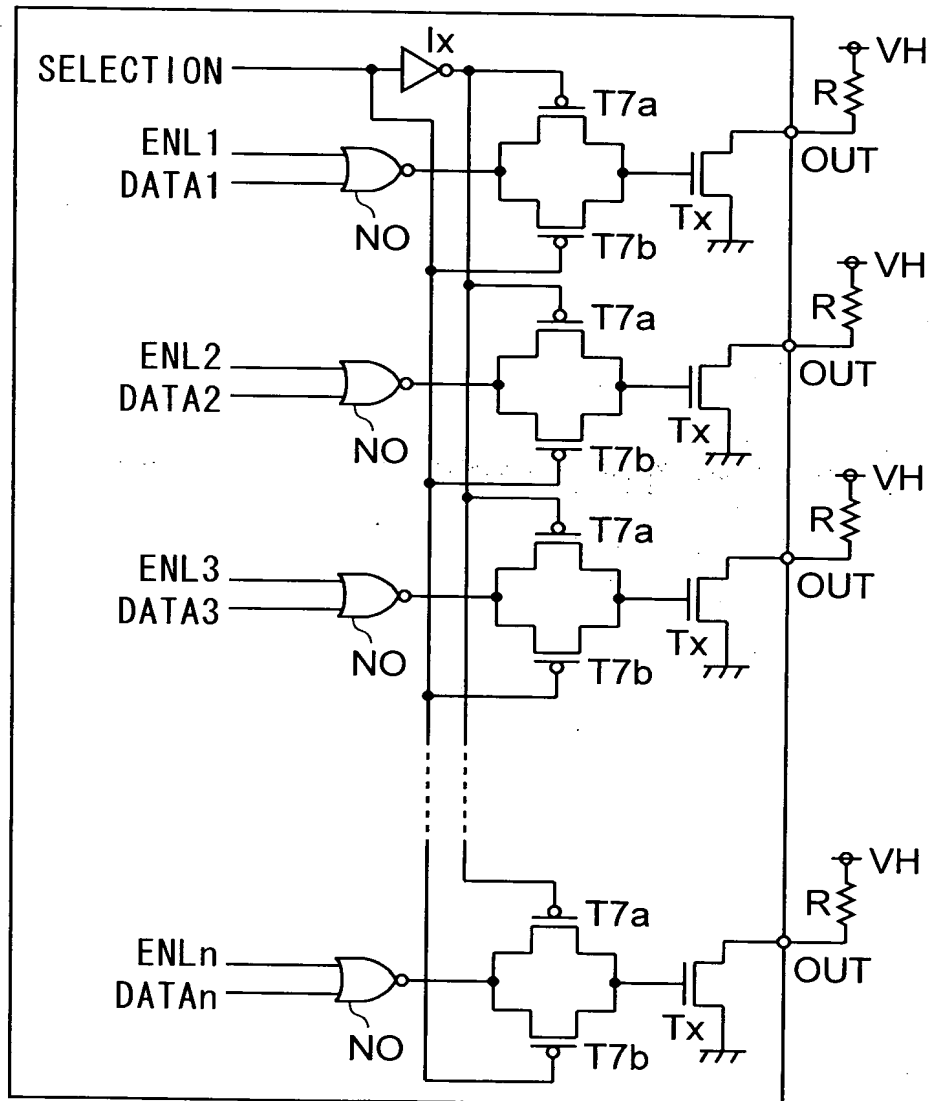


FIG.6



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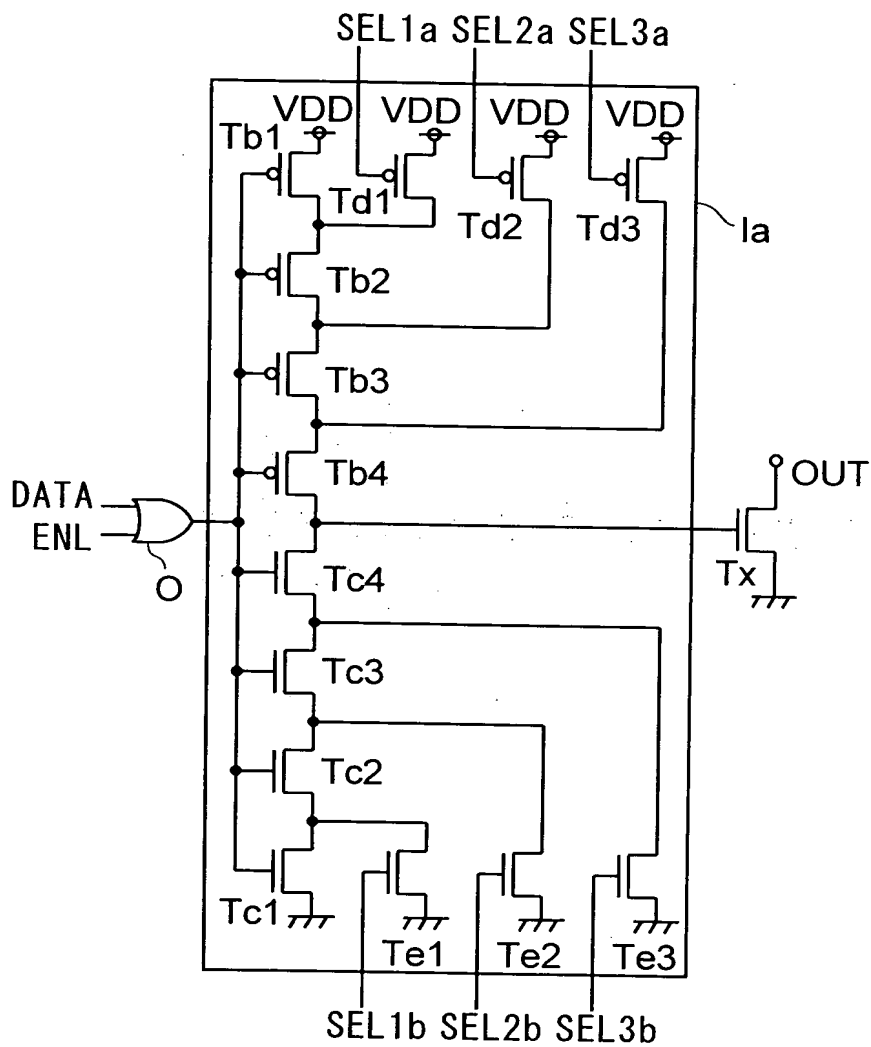
FIG.7



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FIG.8



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FIG.9

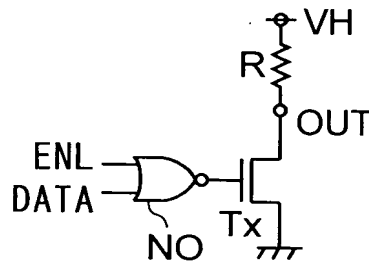
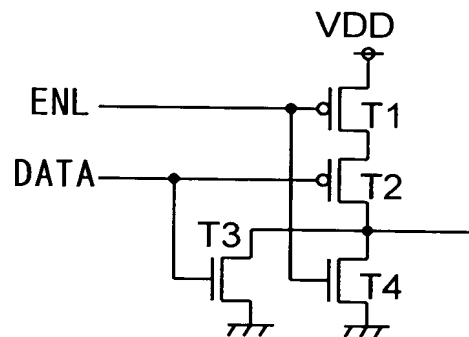


FIG.10



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FIG.11

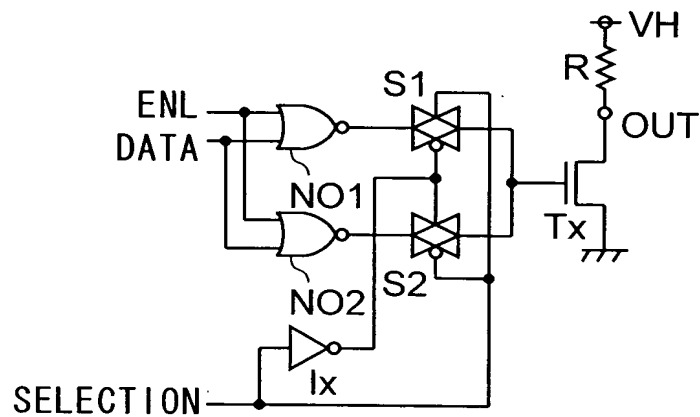
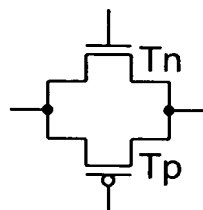


FIG.12



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